Amendments to the Claims

1. (currently amended) A transconductance cell comprising:

a first resistor having a first terminal and a second terminal;

a first half-circuit including:

a first feedback loop wherein the first feedback loop includes a first input transistor receiving a first input voltage at its gate and having a source coupled to the first terminal of the first resistor, a first output transistor having a source coupled to the first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain

wherein the operation of the first feedback loop causes V_{GS} of the first input transistor to remain substantially constant; and

a second half-circuit including:

a second feedback loop wherein the second feedback loop includes a second input transistor receiving a second input voltage at its gate and having a source coupled to the second terminal of the first resistor, a second output transistor having a source coupled to the second terminal of the first resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain

wherein the operation of the second feedback loop causes V_{GS} of the second input transistor to remain substantially constant.

2. (original) The transconductance cell of claim 1, wherein the first input voltage is a positive input voltage and the first output current is a negative output current and the second input voltage is a negative input voltage and the second output current is a positive output current.

3. (original) The transconductance cell of claim 1, further comprising:

a first current source coupled to the drain of the first input transistor; and

a second current source coupled to the drain of the second input transistor.

4. (original) The transconductance cell of claim 1, further comprising:

a first impedance coupled to the drain of the first input transistor; and

a second impedance coupled to the drain of the second input transistor.

5. (currently amended) A transconductance cell comprising: ~~The transconductance cell of claim 4,~~

a first resistor having a first terminal and a second terminal;

a first half-circuit including:

a first feedback loop wherein the first feedback loop includes a first input transistor receiving a first input voltage at its gate and having a source coupled to the first terminal of the first resistor, a first output transistor having a source coupled to the first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain; and

a second half-circuit including:

a second feedback loop wherein the second feedback loop includes a second input transistor receiving a second input voltage at its gate and having a source coupled to the second terminal of the first resistor, a second output transistor having a source coupled to the second terminal of the first resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain,

a first impedance coupled to the drain of the first input transistor; and

a second impedance coupled to the drain of the second input transistor,

wherein the first impedance comprises a resistor and the second impedance comprises a resistor.

6. (original) The transconductance cell of claim 1, further comprising:

a first bias current source coupled to the first terminal of the first resistor; and

a second bias current source coupled to the second terminal of the first resistor.

7. (original) The transconductance cell of claim 1, wherein a well of the first input transistor and a well of the second input transistor are coupled to their respective sources.

8. (original) The transconductance cell of claim 1, wherein the first input transistor and the second input transistor are of the same polarity.

9. (original) The transconductance cell of claim 1, wherein the first output transistor and the second output transistor are of the same polarity.

10. (original) The transconductance cell of claim 1, wherein the first input transistor and the second input transistor are PMOS transistors.

11. (original) The transconductance cell of claim 1, wherein the first output transistor and the second output transistor are PMOS transistors.

12. (original) The transconductance cell of claim 3, wherein the first half-circuit further comprises a third current source coupled to the drain of the first output transistor and the second half-circuit further comprises a fourth current source coupled to the drain of the second output transistor.

13. (original) The transconductance cell of claim 3, wherein the first current source comprises a first current source transistor and the second current source comprises a second current source transistor, and

wherein the drain of the first current source transistor is coupled to the drain of the first input transistor and the drain of the second current source transistor is coupled to the drain of the second input transistor.

14. (original) The transconductance cell of claim 13, wherein the first and second current source transistors have a common polarity.

15. (original) The transconductance cell of claim 14, wherein the first and second current source transistors are NMOS transistors.

16. (currently amended) A transconductance cell comprising:

a first half-circuit including:

a first resistor, and

a first feedback loop wherein the first feedback loop includes a first input transistor receiving a first input voltage at its gate, a first output transistor having a source coupled to a source of the first input transistor and a first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain

wherein the operation of the first feedback loop causes V_{GS} of the first input transistor to remain substantially constant; and

a second half-circuit including:

a second resistor having a first terminal coupled to a second terminal of the first resistor, and

a second feedback loop wherein the second feedback loop includes a second input transistor receiving a second input voltage at its gate, a second output transistor having a source coupled to a source of the second input transistor and a second terminal of the second resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain,

wherein the operation of the second feedback loop causes V_{GS} of the second input transistor to remain substantially constant.

17. (original) The transconductance cell of claim 16, wherein the first input voltage is a positive input voltage and the first output current is a negative output current and the second input voltage is a negative input voltage and the second output current is a positive output current.

18. (original) The transconductance cell of claim 16, further comprising:

a first current source coupled to the drain of the first input transistor; and

a second current source coupled to the drain of the second input transistor.

19. (original) The transconductance cell of claim 16, further comprising:

a first impedance coupled to the drain of the first input transistor; and

a second impedance coupled to the drain of the second input transistor.

20. (original) The transconductance cell of claim 19, wherein the first impedance comprises a resistor and the second impedance comprises a resistor.

21. (original) The transconductance cell of claim 16, further comprising a bias current source coupled to the second terminal of the first resistor and the first terminal of the second resistor.

22. (original) The transconductance cell of claim 16, further comprising:

a first bias current source coupled to the first terminal of the first resistor; and

a second bias current source coupled to the second terminal of the second resistor.

23. (original) The transconductance cell of claim 16, further comprising:

a first bias current source coupled to the second terminal of the first resistor and the first terminal of the second resistor;

a second bias current source coupled to the first terminal of the first resistor; and

a third bias current source coupled to the second terminal of the second resistor.

24. (original) The transconductance cell of claim 16, wherein a well of the first input transistor and a well of the second input transistor are coupled to their respective sources.

25. (original) The transconductance cell of claim 18 wherein the first half-circuit further comprises a third current source coupled to the drain of the first output transistor and the second half-circuit further comprises a fourth current source coupled to the drain of the second output transistor.

26. (original) The transconductance cell of claim 18, wherein the first current source comprises a first current source transistor coupled in series with a third resistor and the second current source comprises a second current source transistor coupled in series with a fourth resistor,

wherein the drain of the first current source transistor is coupled to the drain of the first input transistor and the drain of the second current source transistor is coupled to the drain of the second input transistor.

27. (original) The transconductance cell of claim 26, further comprising a capacitor coupled to a gate of the first and second current source transistors.

28. (original) The transconductance cell of claim 18, wherein the first current source comprises a first current source transistor and the second current source comprises a second current source transistor, and

wherein the drain of the first current source transistor is coupled to the drain of the first input transistor and the drain of the second current source transistor is coupled to the drain of the second input transistor.

29. (currently amended) An analog circuit comprising:

a low noise transconductance cell having a first output node and a second output node, wherein the low noise transconductance cell comprises:

a first half-circuit including:

a first resistor, and

a feedback loop wherein the feedback loop includes a first input transistor receiving a first input voltage at its gate, a first output transistor having a source coupled to a source of the first input transistor and a first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain;

a second half-circuit including:

a second resistor having a first terminal coupled to a second terminal of the first resistor, and

a feedback loop wherein the feedback loop includes a second input transistor receiving a second input voltage at its gate, a second output transistor having a source coupled to a source of the second input transistor and a second terminal of the second resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain; and

a bias current source coupled to the second terminal of the first resistor and the first terminal of the second resistor;

a high swing transconductance cell having a first output node and a second output node; and

an output switch having a first input node coupled to the first output node of the low noise transconductance cell, a second input node coupled to the second output node of the low noise transconductance cell, a third input node coupled to the first output node of the high swing transconductance cell, and a fourth input node coupled to the second output node of the high swing transconductance cell,

wherein a first and a second output node of the output switch are coupled to the first and second input nodes of the output switch when the low noise transconductance cell is selected and the first and second output nodes of the output switch are coupled to the third and fourth input nodes of the output switch when the high swing transconductance cell is selected.

30. (original) The analog circuit of claim 29, wherein the high swing transconductance cell comprises:

a first resistor having a first terminal and a second terminal;

a first half-circuit including:

a feedback loop wherein the feedback loop includes a first input transistor receiving a first input voltage at its gate and having a source coupled to the first terminal of the first resistor, a first output transistor having a source coupled to the first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain;

a second half-circuit including:

a feedback loop wherein the feedback loop includes a second input transistor receiving a second input voltage at its gate and having a source coupled to the second terminal of the first resistor, a second output transistor having a source coupled to the second terminal of the first resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain;

a first bias current source coupled to the first terminal of the first resistor; and

a second bias current source coupled to the second terminal of the first resistor.

31. (canceled)

32. (original) The analog circuit of claim 29 wherein the high swing transconductance cell comprises:

a first half-circuit including:

a first resistor, and

a feedback loop wherein the feedback loop includes a first input transistor receiving a first input voltage at its gate, a first output transistor having a source coupled to a source of the first input transistor and a first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain;

a second half-circuit including:

a second resistor having a first terminal coupled to a second terminal of the first resistor, and

a feedback loop wherein the feedback loop includes a second input transistor receiving a second input voltage at its gate, a second output transistor having a source coupled to a source of the second input transistor and a second terminal of the second resistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain;

a first bias current source coupled to the first terminal of the first resistor; and

a second bias current source coupled to the second terminal of the second resistor.

33. (currently amended) A transconductance cell comprising:

a first half-circuit including:

a first resistor, and

a first feedback loop coupled to a first terminal of the first resistor, wherein the first feedback loop includes a first inverter stage, ~~having~~ a first input transistor having a drain coupled to an input of the first inverter stage and a first output transistor having a gate coupled to an output of the first inverter stage, wherein the first feedback loop is configured to keep V_{GS} of the first input transistor constant;

a second half-circuit including:

a second resistor having a first terminal coupled to a second terminal of the first resistor, and

a second feedback loop coupled to a second terminal of the second resistor, wherein the second feedback loop includes a second inverter stage, ~~having~~ a second input transistor having a drain coupled to an input of the first inverter stage and a first output transistor having a gate coupled to an output of the first inverter stage, ~~coupled to the second resistor~~ wherein the second feedback loop is configured to keep V_{GS} of the second input transistor constant.

34. (original) The transconductance cell of claim 33, further comprising

a first current source coupled to the first input transistor; and

a second current source coupled to the second input transistor.

35. (currently amended) A transconductance cell comprising:

a first resistor having a first terminal and a second terminal;

a first half-circuit including:

a feedback loop ~~having a first input transistor~~ coupled to the first terminal of the first resistor ,wherein the feedback loop includes a first inverter stage, ~~having~~ a first input transistor having a drain coupled to an input of the first inverter stage, and a first output transistor having a gate coupled to an output of the first inverter stage, wherein the feedback loop is configured to keep V_{GS} of the first input transistor constant; and

a second half-circuit including:

a feedback loop ~~having a second input transistor~~ coupled to the second terminal of the first resistor , wherein the feedback loop includes a second inverter stage, ~~having~~ a second input transistor having a drain coupled to an input of the first inverter stage, and a first output transistor having a gate coupled to an output of the first inverter stage, wherein the feedback loop is configured to keep V_{GS} of the second input transistor constant.

36. (original) The transconductance cell of claim 35, further comprising

a first current source coupled to the first input transistor; and

a second current source coupled to the second input transistor.

37. (original) A transconductance cell comprising:

a first feedback loop wherein the feedback loop includes:

a first input transistor receiving a first input voltage at its gate,

a first amplifier having a positive terminal and a negative terminal, wherein the negative terminal is coupled to a drain of the first input transistor,

a first floating voltage source having a first end coupled to a source of the first input transistor and a second end coupled to the positive terminal of the amplifier, and

a first output transistor having a gate coupled to an output of the amplifier, wherein the first output transistor provides a first output current at its drain; and

a second feedback loop wherein the feedback loop includes:

a second input transistor receiving a second input voltage at its gate,

a second amplifier having a positive terminal and a negative terminal, wherein the negative terminal is coupled to a drain of the second input transistor,

a second floating voltage source having a first end coupled to a source of the second input transistor and a second end coupled to the positive terminal of the amplifier, and

a second output transistor having a gate coupled to an output of the amplifier, wherein the second output transistor provides a second output current at its drain.

38. (original) The transconductance cell of claim 37, wherein the first input voltage is a positive input voltage and the first output current is a negative output current and the second input voltage is a negative input voltage and the second output current is a positive output current.

39. (currently amended) A transconductance cell comprising:

a first half-circuit including:

a first feedback loop wherein the first feedback loop includes a first input transistor receiving a first input voltage at its gate and having a source, a first output transistor having a source coupled to the source of the first input transistor, and an inverter stage having an input coupled to a drain of the first input transistor and an output coupled to a gate of the first output transistor, wherein the first output transistor provides a first output current at its drain

wherein the operation of the first feedback loop causes V_{GS} of the first input transistor to remain substantially constant;

a second half-circuit including:

a second feedback loop wherein the second feedback loop includes a second input transistor receiving a second input voltage at its gate and having a source, a second output transistor having a source coupled to the source of the second input transistor, and an inverter stage having an input coupled to a drain of the second input transistor and an output coupled to a gate of the second output transistor, wherein the second output transistor provides a second output current at its drain

wherein the operation of the second feedback loop causes V_{GS} of the second input transistor to remain substantially constant; and

a plurality of switchable resistance stages.

40. (original) The transconductance cell of claim 39, wherein one of the plurality of switchable resistance stages is coupled between the first feedback loop and the second feedback loop when the first, second, third, and fourth switches are closed.

41. (original) The transconductance cell of claim 39 further comprising a resistor coupled to the source of the first input transistor and to the source of the second input transistor.

42. (original) The transconductance cell of claim 39, further comprising:

a current source coupled to a first terminal of a fifth switch, wherein a second terminal of the fifth switch is coupled to one of the plurality of resistance stages.

43. (original) The transconductance cell of claim 42, wherein the current source is coupled to one of the plurality of resistance stages when the fifth switch is closed.

44. (currently amended) A transconductance cell comprising:

a first resistance stage, wherein the first resistance stage includes:

a first resistor having a first and a second terminal,

a second resistor having a first and a second terminal, and

a first switch wherein a first terminal of the first switch is coupled to the second terminal of the first resistor and a second terminal of the first switch is coupled to the second terminal of the second resistor;

a second resistance stage, wherein the second resistance stage includes:

a third resistor having a first and a second terminal,

a fourth resistor having a first and a second terminal, and

a second switch wherein a first terminal of the second switch is coupled to the second terminal of the third resistor and a second terminal of the second switch is coupled to the second terminal of the fourth resistor; and

a first feedback loop coupled to the first terminal of the third resistor and the first terminal of the first resistor; ~~and~~

a second feedback loop coupled to the first terminal of the fourth resistor and the first terminal of the second resistor ;

a first current source coupled to a first terminal of a third switch; and

a second current source coupled to a first terminal of a fourth switch,

wherein a second terminal of the third switch is coupled to the first feedback loop and a third terminal of the third switch is coupled to the second terminal of the first resistor in the first resistance stage, and

wherein a second terminal of the fourth switch is coupled to the second feedback loop and a third terminal of the fourth switch is coupled to the second terminal of the second resistor in the second resistance stage.

45. (original) The transconductance cell of claim 44, wherein the first resistance stage is coupled between the first feedback loop and the second feedback loop when the first switch is closed.

46. (original) The transconductance cell of claim 44, wherein the second resistance stage is coupled between the first feedback loop and the second feedback loop when the second switch is closed.

47. (original) The transconductance cell of claim 44 further comprising a resistor coupled to the first feedback loop and to the second feedback loop.

48. (canceled)

49. (currently amended) [[A]] The transconductance cell of claim 39, wherein each of the ~~comprising:~~ [[a]] plurality of resistance stages [[,]] ~~wherein each resistance stage~~ includes:

a first resistor having a first and a second terminal,

a second resistor having a first and a second terminal, and

a first switch wherein a first terminal of the first switch is coupled to the second terminal of the first resistor and a second terminal of the first switch is coupled to the second terminal of the second resistor [[;]]

~~a first feedback loop coupled to the first terminal of the first resistor in each of the plurality of resistance stages; and~~

~~a second feedback loop coupled to the first terminal of the second resistor in each of the plurality of resistance stages~~.

50. (currently amended) A transconductance cell comprising:

a resistor having a first and a second terminal; and

a feedback loop wherein the feedback loop includes [[a]] ~~first~~ an input transistor receiving an input voltage at its gate and having a source coupled to the first terminal of the first resistor, [[a]] ~~first~~ an output transistor having a source coupled to the first terminal of the first resistor, and an inverter stage having an input coupled to a drain of the ~~first~~ input transistor and an output coupled to a gate of the ~~first~~ output transistor, wherein the first output transistor provides an output current at its drain

wherein the operation of the feedback loop cause V_{GS} of the input transistor to remain substantially constant.

51. (original) The transconductance cell of claim 39, wherein each of the plurality of switchable resistance stages includes a resistance wherein a first end of the resistance is coupled to a first terminal of a first switch and to a first terminal of a second switch and a second end of the resistance is coupled to a first terminal of a third switch and to a first terminal of a fourth switch, and wherein the second terminal of the first switch is coupled to the source of the first input transistor, the second terminal of the second switch is coupled to the source of first output terminal, the second terminal of the third switch is coupled to the source of the second input transistor, and the second terminal of the fourth switch is coupled to the source of the second output transistor.

52. (new) The transconductance cell of claim 4, wherein the first impedance comprises a resistor and the second impedance comprises a resistor.